AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A method for forming an electronic device having a multilayer structure, comprising:

embossing a surface of a substrate so as to depress first and second regions of the substrate relative to at least a third region of the substrate;

treating the surface of the substrate with a surface modification process that has a different effect on depressed regions of the substrate relative to non-depressed regions of the substrate, whereby the non-depressed regions and the depressed regions are given different surface energies, such that the deposition of a material is defined by the surface energy of the substrate in the first and second regions

~~applying a solution of a~~ depositing conductive or semiconductive material from solution onto the first and second regions of the substrate so as to ~~confine in a single step the deposition of said conductive or semiconductive material to said first and second regions , whereby the conductive or semiconductive material~~ [[forms]] form a first electrode on the first region and a second electrode on the second region, wherein the first and second electrodes are electrically insulated from each other by the third region; and wherein the third region is a ridge wherein the ridge has a width that defines a length of a channel of the electronic device.

2. (previously presented): A method as claimed in claim 1, wherein the third region has a width defined by a depth to which embossing is performed.

3. (previously presented): A method as claimed in claim 2, wherein the step of embossing is performed with a tool having an embossing surface, the embossing surface of the tool bearing at least one protruding portion having a sharp protruding tip wherein the protruding portion has a width that widens from the sharp protruding tip, towards the embossing surface of

the tool such that the width of a depressed region of the substrate, as measured in a plane of the surface of the substrate, is dependent on a depth to which the at least one protruding portion of the tool enters into the substrate.

4. (currently amended): A method as claimed in claim 2, wherein the step of embossing is performed with a tool having an embossing surface, the embossing surface of the tool bearing at least one recessed portion having a recessed point wherein the recessed portion has a width that widens from the recessed point, towards the embossing surface of the tool such that a raised region of the substrate has a width, as measured in a plane of the surface of the substrate, that is dependent on a depth to which the embossing surface of the tool enters into the substrate.

5. - 6. (cancelled).

7. (currently amended): A method as claimed in claim [[6]] 1, wherein a cross section of the ridge is substantially rectangular.

8. (currently amended): A method as claimed in claim [[6]] 1, wherein a cross section of the ridge is substantially triangular.

9. (previously presented): A method as claimed in claim 1, wherein the embossing step is performed at a temperature within 50 °C of the glass transition temperature of a topmost surface of the substrate.

10. (previously presented): A method as claimed in claim 1, wherein the embossing step is performed at a temperature at which a topmost surface of the substrate is in a liquid phase.

11. (previously presented): A method as claimed in claim 1, wherein the substrate comprises a flexible plastic substrate such as poly(ethyleneterephthalate) (PET), polyethersulphone (PES) or polyethernaphthalene (PEN).

12. (previously presented): A method as claimed in claim 1, wherein the substrate comprises a rigid substrate coated with a polymer layer.

13. (currently amended) A method as claimed in claim [[5]] 1, wherein said substrate~~treating step~~ comprises ~~using~~ a polar polymer layer ~~having a high surface energy~~ as the substrate.

14. (currently amended): A method as claimed in claim [[5]] 1, wherein said treating step comprises exposing the substrate to one or more of an oxygen plasma, carbon-tetrafluoride plasma, ultra-violet or ozone surface treatment.

15. (currently amended): A method as claimed in claim [[5]] 1, wherein said treating step comprises depositing a surface modifying layer onto the substrate at an oblique angle such that the surface modifying material is deposited onto the non-depressed portions of the substrate, and the depressed portions are shadowed by the non-depressed portions during the deposition of the surface modifying layer.

16. (currently amended): A method as claimed in claim [[5]] 1, wherein said treating step comprises exposing the substrate to a physical etching method such as reactive ion etching.

17. (currently amended): A method as claimed in claim [[5]] 1, wherein said treating step comprises applying a flat stamp to the surface.

18. (original): A method as claimed in claim 17, wherein the flat stamp is inked with a self-assembled monolayer.

19. (original): A method as claimed in claim 18, wherein the self-assembled monolayer is capable of bonding with functional groups on the surface of the substrate.

20. (previously presented): A method as claimed in claim 18, wherein the self-assembled monolayer is octyltrichlorosilane or fluoroalkyltrichlorosilane.

21. (original): A method as claimed in claim 18, wherein the self-assembled monolayer comprises a methoxy silane.

22. (previously presented): A method as claimed in claim 1, wherein the solution of conductive or semiconductive material comprises a conductive ink.

23. (original): A method as claimed in claim 22, wherein the conductive ink comprises a conductive polymer.

24. (original): A method as claimed in claim 23, wherein the conductive polymer is polyethylenedioxythiophene doped with polystyrene sulfonic acid (PEDOT/PSS).

25. (original): A method as claimed in claim 22, wherein the conductive ink comprises a conductive inorganic dispersion of electrically conductive nanoparticles.

26. (cancelled).

27. (previously presented): A method as claimed in claim 1, further comprising the step of depositing a layer of semiconductive material over the substrate and first and second electrodes.

28. (previously presented): A method as claimed in claim 27, wherein the semiconductive material formed over the substrate and first and second electrodes is regioregular poly(3-hexylthiophene) (P3HT) or poly(dioctylfluorene-co-bithiophene) (F8T2).

29. (previously presented): A method as claimed in claim 27, wherein the semiconductive material formed over the substrate and first and second electrodes is an inorganic nanoparticulate or an inorganic nanowire semiconductor. .

30. (currently amended): A method as claimed in <u>one of claims</u> [[claim]] 27 to 29, further comprising the step of depositing a layer of dielectric over the layer of semiconductive material.

31. (original): A method as claimed in claim 30, wherein the layer of dielectric comprises a polymer layer.

32. (previously presented): A method as claimed in claim 31, wherein the polymer layer is poly(methylmethacrylate) (PMMA).

33. (previously presented): A method as claimed in claim 29, further comprising the step of printing a pattern of conductive material to form an electrode for said electronic device.

34. (original): A method as claimed in claim 33, wherein the electrode is formed from a conductive polymer or an inorganic material.

35. (cancelled).

36. (previously presented): A method as claimed in claim 1, wherein the electronic device is a transistor.

37. (previously presented): A method as claimed in claim 1, wherein conductive material is deposited on the substrate which forms source and drain electrodes of the electronic device.

38. (previously presented): A method as claimed in claim 30, wherein the layer of dielectric deposited over the semiconductive layer is a gate dielectric layer.

39. (original): A method as claimed in claim 38, further comprising the step of depositing a gate electrode onto the surface of the gate dielectric layer.

40. (previously presented): A method as claimed in claim 1, wherein the embossing step is performed with a tool having an embossing surface suitable for embossing the substrate, the embossing surface bearing an array of protruding features with sharp tips.

41. (previously presented): A method as claimed in claim 40, wherein the sharp tips have a radius of curvature of less than 100 μm.

42. (previously presented): A method as claimed in claim 40, wherein the sharp tips have a radius of curvature of less than 10 μm.

43. (original): A method as claimed in claim 40, wherein the protruding features have a rectangular profile.

44. (previously presented): A method as claimed in claim 1, wherein the third region has a width of less than 20 μm.

45. (previously presented): A method as claimed in claim 1, wherein the third region has a width of less than 5 μm.

46. (previously presented): A method as claimed in claim 1, wherein the third region has a width of less than 1 μm.

47. (previously presented): A method as claimed in claim 1, wherein the substrate comprises a functional layer of the electronic device, wherein the functional layer comprises one of a conducting material and a semiconducting material.

48. – 122. (cancelled).

123. (previously presented): A method as claimed in claim 1, wherein the first and second electrodes are source and drain electrodes of a transistor.